WE CLAIM:

1. Apparatus for processing data, said apparatus comprising:

a register bank having one or more registers operable to hold respective data values;

a data access circuit operable to perform data access operations transferring one or more data values between said apparatus and addressed memory locations within a memory circuit; and

an instruction decoder responsive to data access program instructions to control said data access circuit to perform respective data access operations, each of said data access program instructions including an address offset field that specifies an offset value and including a base register field that specifies a base address register within said register bank and specifying a manipulation to be performed upon said offset value and a base address value held in said base address register to form a memory address value to be accessed within said memory circuit upon execution of said data access program instruction; wherein

said data access program instructions have:

(i) a first form including an address offset field having a first address offset field length; and

(ii) a second form including an address offset field having a second address offset field length, said first address offset field length being greater than said second address offset field length and said first form being capable of specifying a lesser number of possible manipulations to be performed upon said base address value and said offset value than said second form.

2. Apparatus as claimed in claim 1, wherein said manipulation forms a modified address value by one out of:

adding said offset value to said base address value; and

subtracting said offset value from said base address value.

3. Apparatus as claimed in claim 1, wherein said manipulation also allows at least one of the following options for a data access operation:

using said base address value as said memory address value;

using said modified address value as said memory address value;

using said base address value and writing back said modified address value to said base address register as said memory address value; and

using said modified address value and writing back said modified address value to said base address register as said memory address value.

4. Apparatus as claimed in claim 1, wherein said apparatus can operate in a plurality of modes at least one of which is privileged and at least one of which is unprivileged, data accesses being marked either privileged or unprivileged to allow code to be given different levels of access to said memory circuit.

5. Apparatus as claimed in claim 4, wherein at least one form of said manipulation allows a memory access to be forced to be unprivileged regardless of the current mode.

6. Apparatus as claimed in claim 1, wherein data access program instructions of said first form operate with a fixed manipulation in which a sum of said base address value and said offset value is used as said memory address value and said base address value is unchanged after execution.

7. Apparatus as claimed in claim 1, wherein said data access program instructions of said second form includes a manipulation mode control field specifying which one of a plurality of different manipulations is to be used.

8. Apparatus as claimed in claim 1 wherein the sets of manipulations provided by said first form and said second form are disjoint.

9. Apparatus as claimed in claim 1, wherein said data values are transferred between respective registers of said register bank and said addressed memory locations.

10. A method of processing data, said method comprising the steps of:

holding data values within respective ones of one or more registers of a register bank, said register bank forming part of a data processing apparatus;

performing data access operations with a data access circuit to transfer one or more data values between said data processing apparatus and addressed memory locations within a memory circuit; and

in response to data access program instructions, controlling said data access circuit with an instruction decoder to perform respective data access operations, each of said data access program instructions including an address offset field that specifies an offset value and including a base register field that specifies a base address register within said register bank and specifying a manipulation to be performed upon said offset value and a base address value held in said base address register to form a memory address value to be accessed within said memory circuit upon execution of said data access program instruction; wherein

said data access program instructions have:

(i) a first form including an address offset field having a first address offset field length; and

(ii) a second form including an address offset field having a second address offset field length, said first address offset field length being greater than said second address offset field length and said first form being capable of specifying a lesser number of possible manipulations to be performed upon said base address value and said offset value than said second form.

11. A method as claimed in claim 10, wherein said manipulation forms a modified address value by one out of:

adding said offset value to said base address value; and

subtracting said offset value from said base address value.

12. A method as claimed in claim 10, wherein said manipulation also allows at least one of the following options for a data access operation:

using said base address value as said memory address value;

using said modified address value as said memory address value;

using said base address value and writing back said modified address value to said base address register as said memory address value; and

using said modified address value and writing back said modified address value to said base address register as said memory address value.

13. A method as claimed in claim 10, wherein said method is operable in a plurality of modes at least one of which is privileged and at least one of which is unprivileged, data accesses being marked either privileged or unprivileged to allow code to be given different levels of access to said memory circuit.

14. A method as claimed in claim 13, wherein at least one form of said manipulation allows a memory access to be forced to be unprivileged regardless of the current mode.

15. A method as claimed in claim 10, wherein data access program instructions of said first form operate with a fixed manipulation in which a sum of said base address value and said offset value is used as said memory address value and said base address value is unchanged after execution.

16. A method as claimed in claim 10, wherein said data access program instructions of said second form includes a manipulation mode control field specifying which one of a plurality of different manipulations is to be used.

17. A method as claimed in claim 10, wherein the sets of manipulations provided by said first form and said second form are disjoint.

18. A method as claimed in claim 10, wherein said data values are transferred between respective registers of said register bank and said addressed memory locations.

19. A computer program product having a computer program operable to control a data processing apparatus, said computer program holding one or more data values for

manipulation within respective ones of one or more registers of a register bank, and comprising:

data access code operable to perform data access operations with a data access circuit to transfer one or more data values between said data processing apparatus and addressed memory locations within a memory circuit; wherein

said data access code includes a plurality of data access program instructions, each of said data access program instructions including an address offset field that specifies an offset value and including a base register field that specifies a base address register within said register bank and specifying a manipulation to be performed upon said offset value and a base address value held in said base address register to form a memory address value to be accessed within said memory circuit upon execution of said data access program instruction; wherein

said data access program instructions include at least one data access program instruction of each of:

(i) a first form including an address offset field having a first address offset field length; and

(ii) a second form including an address offset field having a second address offset field length, said first address offset field length being greater than said second address offset field length and said first form being capable of specifying a lesser number of possible manipulations to be performed upon said base address value and said offset value than said second form.

20. A computer program product as claimed in claim 19, wherein said manipulation forms a modified address value by one out of:

adding said offset value to said base address value; and

subtracting said offset value from said base address value.

21. A computer program product as claimed in claim 19, wherein said manipulation also allows at least one of the following options for a data access operation:

using said base address value as said memory address value;

using said modified address value as said memory address value;

using said base address value and writing back said modified address value to said base address register as said memory address value; and

using said modified address value and writing back said modified address value to said base address register as said memory address value.

22. A computer program product as claimed in claim 19, wherein said method is operable in a plurality of modes at least one of which is privileged and at least one of which is unprivileged, data accesses being marked either privileged or unprivileged to allow code to be given different levels of access to said memory circuit.

23. A computer program product as claimed in claim 22, wherein at least one form of said manipulation allows a memory access to be forced to be unprivileged regardless of the current mode.

24. A computer program product as claimed in claim 19, wherein data access program instructions of said first form operate with a fixed manipulation in which a sum of said base address value and said offset value is used as said memory address value and said base address value is unchanged after execution.

25. A computer program product as claimed in claim 19, wherein said data access program instructions of said second form includes a manipulation mode control field specifying which one of a plurality of different manipulations is to be used.

26. A computer program product as claimed in claim 19, wherein the sets of manipulations provided by said first form and said second form are disjoint.

27. A computer program product as claimed in claim 19, wherein said data values are transferred between respective registers of said register bank and said addressed memory locations.